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Design and Implementation of a Low Power and Area Efficient Sequential Multiplier

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Abstract
A multiplier plays a major role in various digital systems. The area, speed and power consumption of any digital system, which has a multiplier as its component, depend upon the hardware used for the multiplier. In this paper we proposed a sequential multiplier which has a lower area requirement and lower power consumption in comparison of the conventional sequential multiplier. We can use the proposed system where long battery life is required and/or reduced hardware is required. The speed of the proposed multiplier is a little bit slower than the conventional one. So we can use the proposed system where long battery life is required and speed is not the major requirement.

Keywords- Shift and add multiplier, Controller, Power consumption, Area, Xilinx

1. Introduction

Nowadays more and more complex circuits are implemented on a VLSI chip because the scale of integration keeps increasing continuously. These complex circuits need large signal processing systems, hence require significant amount of power. The two major design tools in VLSI system design are area and power consumption. Power consumption has become an important anxiety in today's VLSI system design. The requirement of low power VLSI design arises from two main factors. First one is the stable growth of operating frequency and processing capability per chip, large currents have to be delivered and the heat due to large power consumption must be removed by proper cooling methods. Second one is that the battery life in portable electronic devices is narrow. Low power design is used to increase the battery backup in these portable devices. Multiplication is an essential operation in most signal processing operations. Multipliers have large area, long intermission and consume substantial amount of power. So low power multiplier design has an important role in low power VLSI system design (Chandrakasan et al., 1992). There has been far-reaching work on low power multiplier design at different levels i.e. technology level, circuit level, physical level, logic levels etc. A multiplier is generally the most area consuming part of a system. Hence by optimizing the area and power of a multiplier, we can optimize the whole system. This is a major design issue. Area and speed are typically incompatible constraints so that improving speed results mostly in larger areas.

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2. Shift-And-Add Method for Multiplication

In designing of multipliers there is always a negotiation to be made between the speed and the area. One of the simplest multiplication methods is shift-and-add method. Shift-and-add method is slow but proficient in use of hardware. In this method, depending on the i^{th} bit of one operand, either another operand is added to the collected partial result and then shifted to the right (if i^{th} is 1), or the collected partial result is shifted to the right by one place without being added to the first operand (if i^{th} bit is 0). This method can be justified by considering manual binary multiplication.

To understand the hardware implementation of this method we make some changes to this method. First, instead of having our inspection point from one bit to another of the operand, we put this operand in a shift register, always observe its right most bit and after each calculation we move it one place to the right, making its next bit available.

Second, instead of writing one partial product and the next one to its left, when we write a partial product, we move it to the right as we are writing it and the next one will not to be shifted.

Finally, instead of calculating all partial product and adding them up at the end, when a partial product is calculated, we add it to the previous partial result and write the newly calculated value as the new partial result (Shen and Chen, 2002).

All these three changes are describes in the example shown in Figure 1 i.e. hardware oriented multiplication process. If the bit being observed of the operand is 0 then there is no need to add anything in the previously calculated partial result and only shifting is sufficient. This process of shifting without adding anything is called “shift”. And if the bit being observed of one operand is 1 then another operand is to be added to the previously calculated partial result and the calculated new partial result should be shifted to the right by one place. This process is called “add-and-shift” (Jayaprakash et al., 2011; Marimuthu et al., 2010).

3. Conventional Sequential Multiplier

The architecture of a conventional sequential multiplier by using shift and add method is shown in Figure 2. There are various major sources of switching activities in this multiplier i.e. shift registers, counter, adder, switching in multiplexer and shifting.

By reducing the switching activity as mentioned above we can design the low power architecture for sequential multiplier. We can reduce these switching activities by using the proposed sequential multiplier architecture.

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4. Proposed Architecture of Sequential Multiplier

If we talk about large digital systems then we have to talk about their data parts and control parts also. To design any large digital system first we have to clarify the design of its datapath and control unit.

The data parts consist of registers, multiplexers, adders and buses interconnecting them. The control unit is a state machine which controls the sequence of operation of the data parts. As shown in Figure 3, the data parts and the control unit both are working on the same clock pulse. On each rising edge the controller goes into a new state and issues various control signals and the parts of the data path starts reacting according to these signals. The time for the data parts to complete their individual task is equal to the time from one rising edge to next rising edge of the clock pulse. Values that are applied at the inputs of the datapath registers are clocked into these registers at every rising edge of the clock pulse (Chen et al., 2003; Moshnyaga and Tamaru, 1995).

Now let us discuss the functioning of the proposed architecture of the sequential multiplier. As shown in the Figure 4 registers P and B are 8 bit registers. A multiplexer, an adder and a tri state buffer amount to the other components of the datpath of the proposed architecture.

In the above figure the signals which are shown in bold are the control signals from the control unit. These control signals control the register clocking, bus assignments and logic unit output selection. To load the multiplier and multiplicand into the registers A and B, the input databus is used. This databus is a bidirectional bus and is driven by the output of P through an actual tri state buffer and by the tri state output of A.

The output of P and B are goes into an adder (8- bit) for the addition of the partial result in P to the B. The output of this adder i.e. P+B, goes to the one side of the multiplexer and the other side of the multiplexer is driven by the P output i.e. P+0. The sel_sum control input decides which input will pass to the output of the multiplexer i.e. P+B or P+0 as shown in Figure 4. The AND gate selects the carry output from the adder or 0 according to the sel_sum control input. This value is concatenated to the left of the multiplexer output and form a 9-bit vector. After this the right most bit of this vector come apart and goes into the sequential input of the shift register that contains A and the other 8-bits goes tom the register P. This concatenation of the AND gate output to the left of the multiplexer output and splitting the right bit from this 9-bit vector produces a shifted result that is clocked into P. And finally we get the result in P and A. Msb 4-bits in register P and lsb 4-bits in register A.

5. Result and Analysis

After understanding the architecture of both conventional and proposed architecture of sequential multiplier, the next step was to implement it. In order to achieve this we write a code in Verilog Hardware Descriptive Language. This code was synthesized by using Xilinx

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14.7 and simulated using Modelsim Simulator as per Table 1 and Table 2. Area utilization, power analysis report and simulation results are shown below Figure 5 and Figure 6.

6. Conclusion

In this paper the architecture for low power and low area sequential multiplier was proposed. Some modifications are done to the conventional multiplier to reduce the switching activities so that the power consumption can be reduced. The results show that there is a reduction of 34 % in power consumption of the proposed architecture. We also analyze the area utilization of conventional and proposed sequential multiplier. We can use the proposed architecture in those applications where low power and/or low area is required.

Parameters	**Conventional [**Kulkarni et al. (2013)**]**	**Proposed**
No of slices	68	36
No of 4-input LUTs	179	55
No of bonded inputs	35	13

Table 1. Area utilization of conventional and proposed architecture

Parameter	**Conventional [**Kulkarni et al. (2013)**]**	**Proposed**
Static Power (mW)	41.70	31.52
Dynamic Power (mW)	8.35	1.30
Total power (mW)	50.12	32.83

Table 2. Power analysis of conventional and proposed architecture

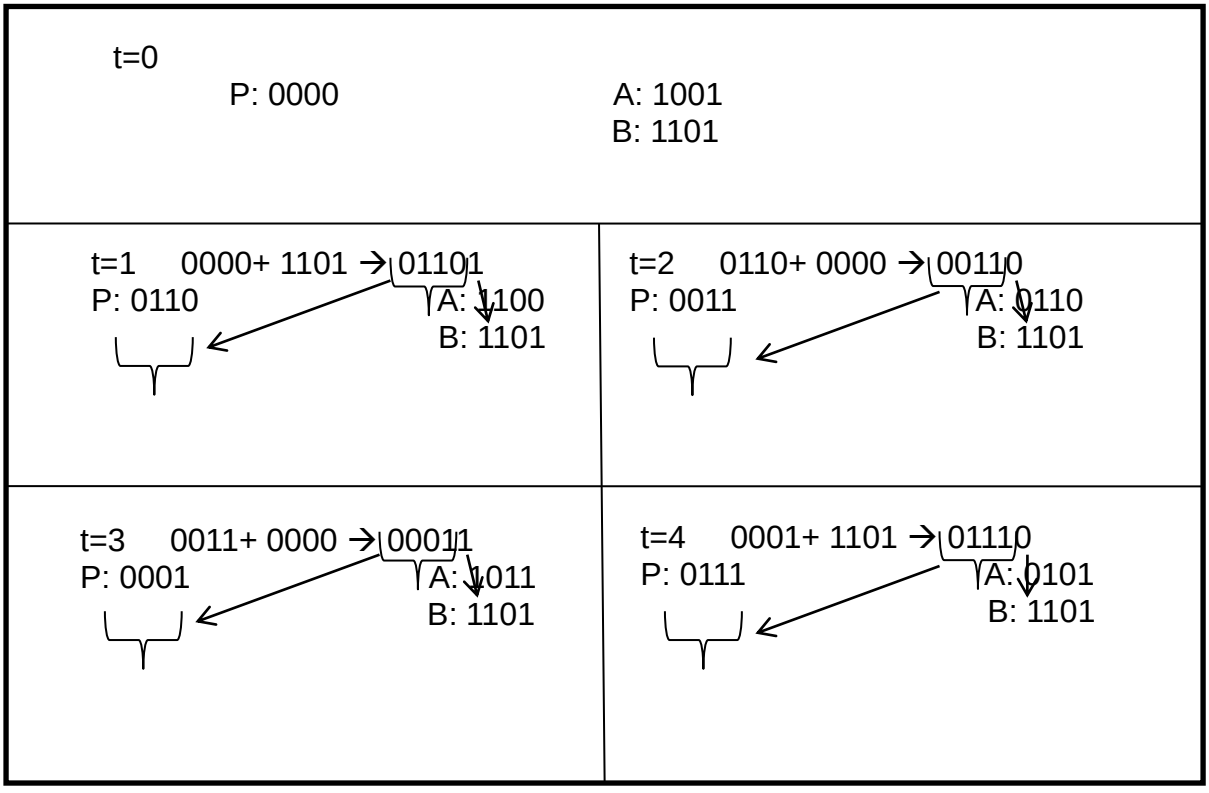

Figure 1. Hardware oriented multiplication process

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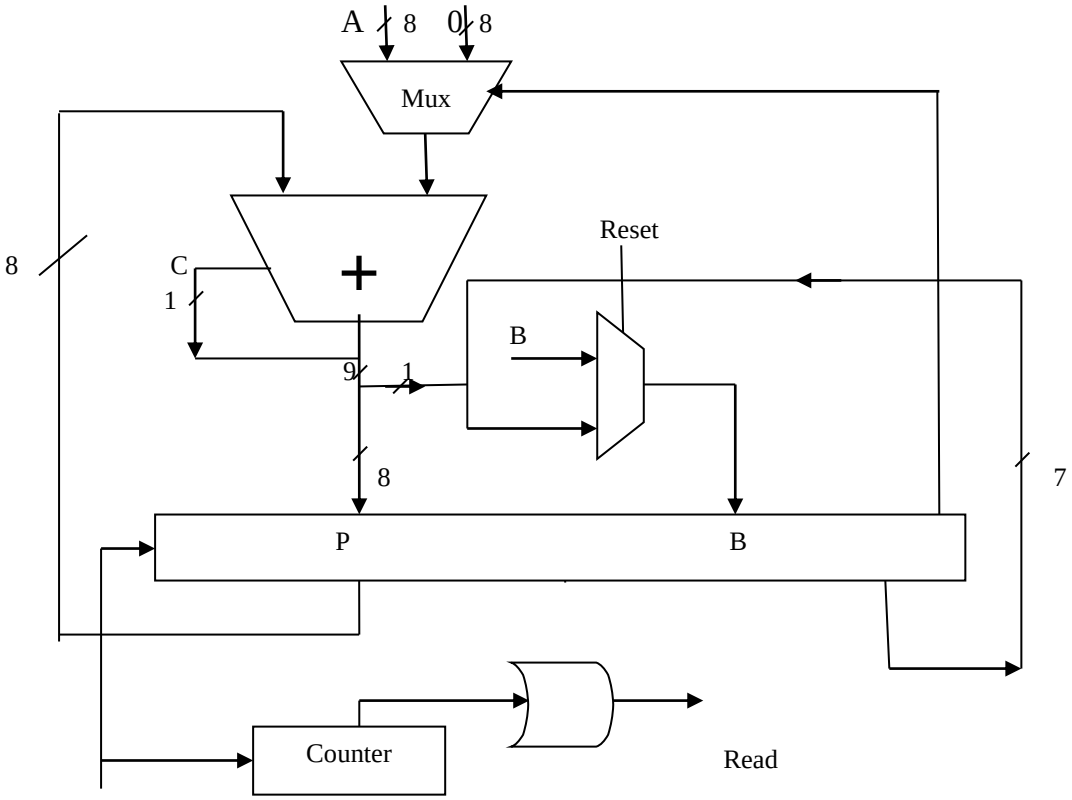

Figure 2. Conventional sequential multiplier

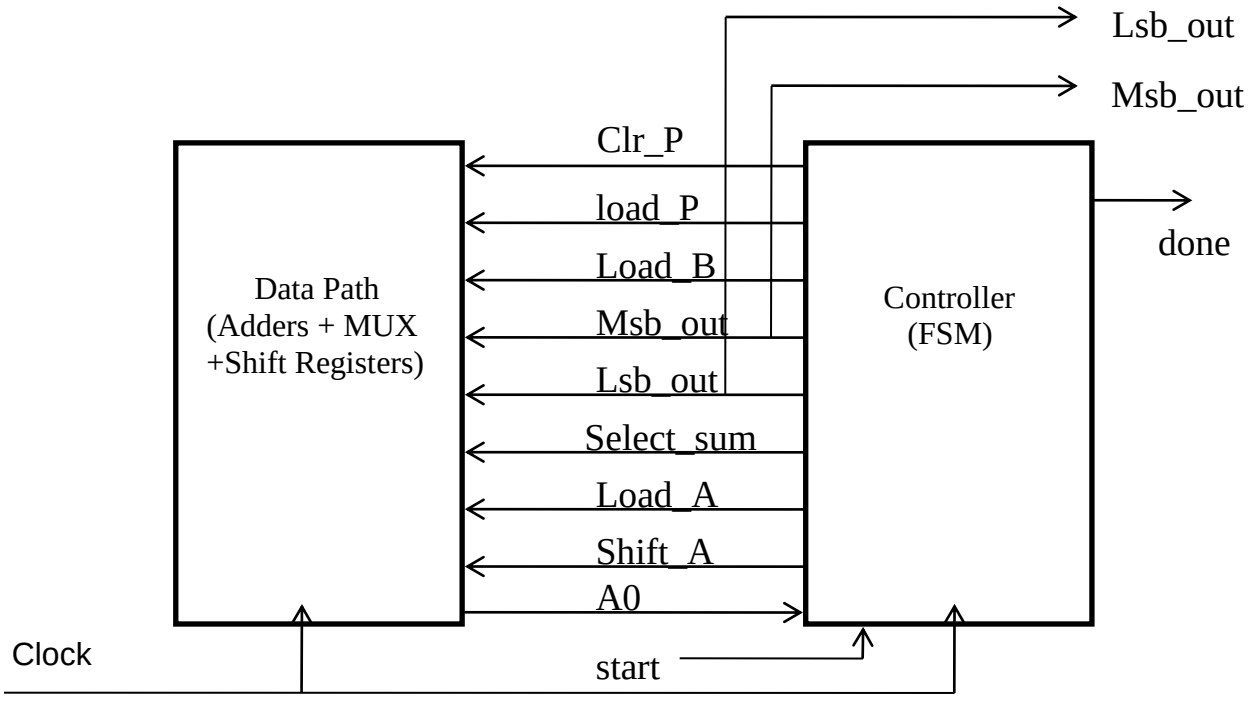

Figure 3. Data and control parts of the proposed architecture

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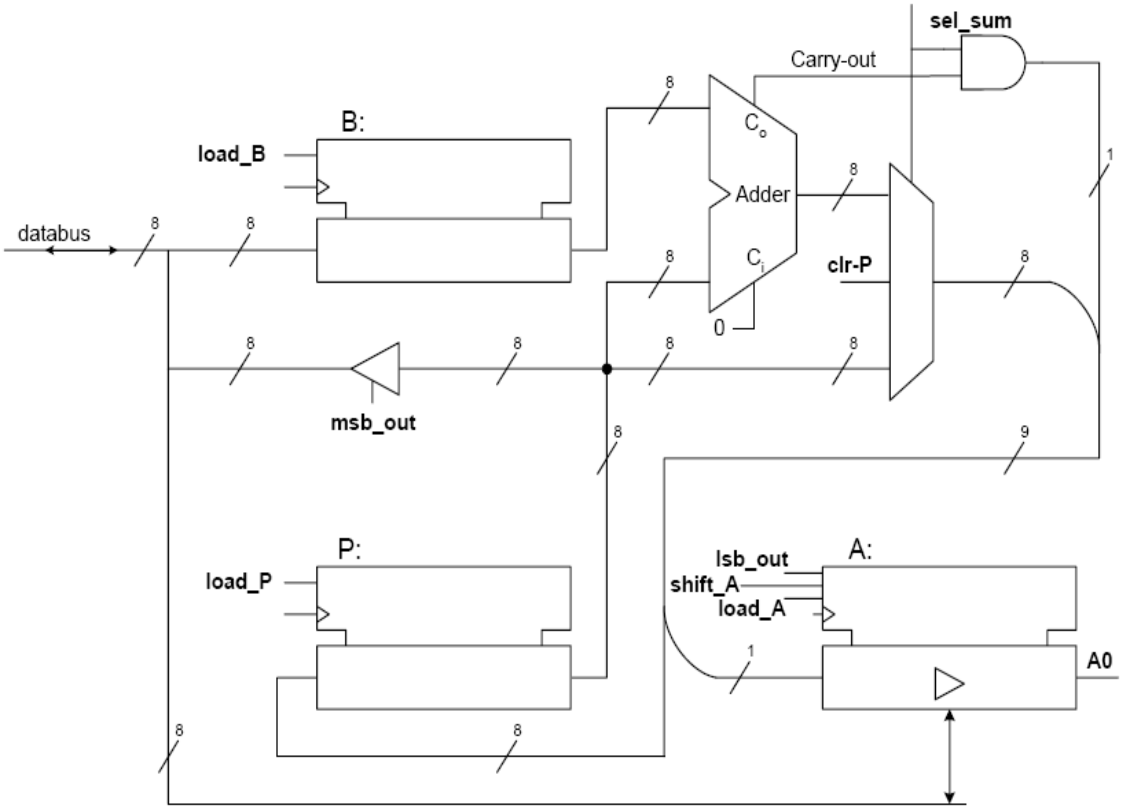

Figure 4. Proposed architecture of sequential multiplier

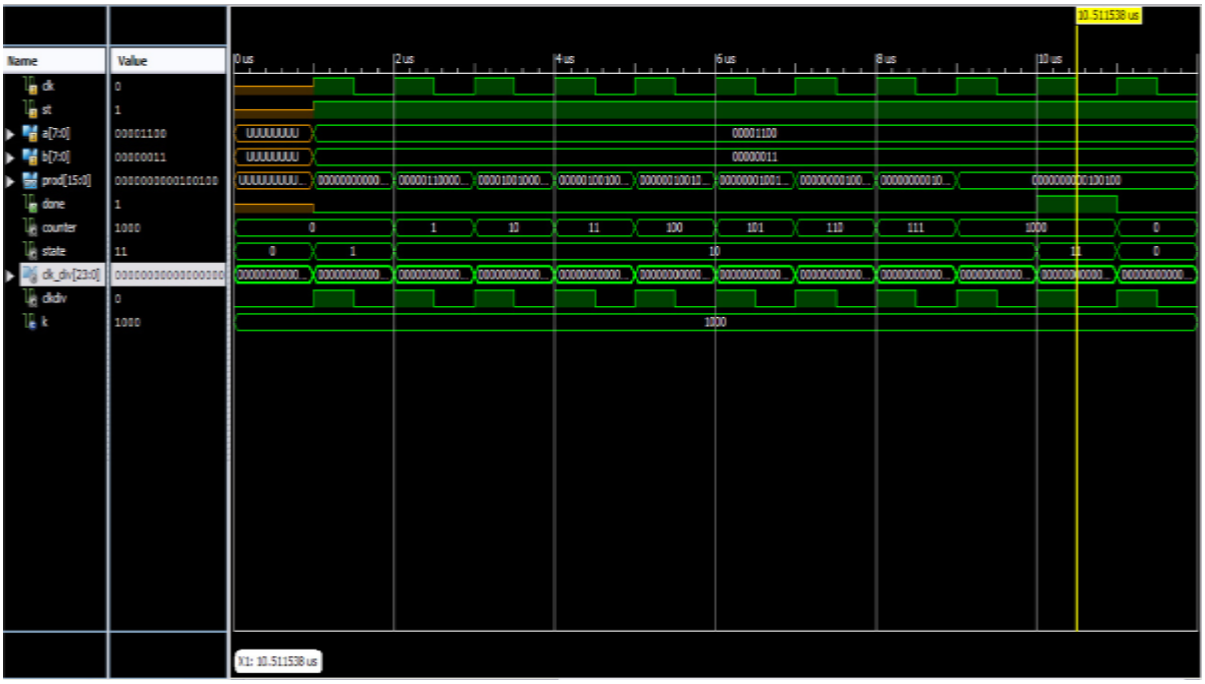

Figure 5. Simulation of 8-bit conventional multiplier [Kulkarni et al. (2013)**]**

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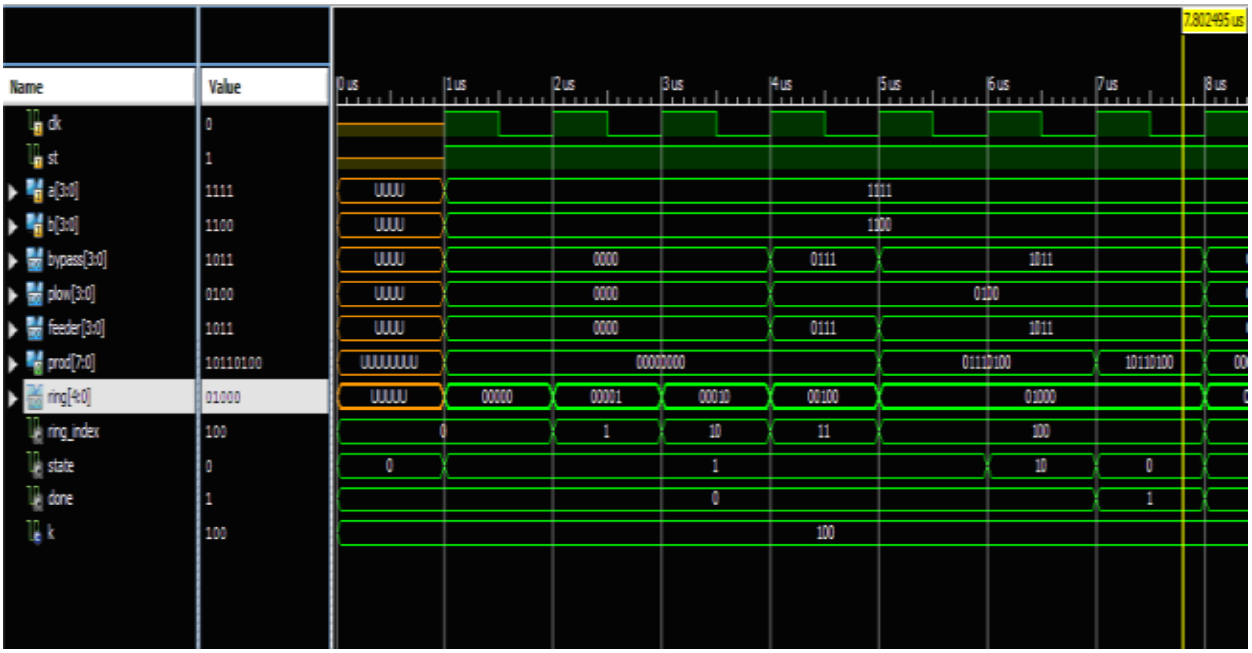

Figure 6. Simulation of 8-bit proposed multiplier

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